# 4 CHANNELS, 24-BIT Σ-Δ ANALOG TO DIGITAL CONVERTER
# (RADIATION HARDENED)

## FEATURES:

- **24 BITS NO MISSING CODES[1]**
- **0.003% INL**
- **19 BITS EFFECTIVE RESOLUTION (PGA = 1, OSR=2048)**
  **12 BITS (PGA = 128, OSR=2048)**
- **PGA FROM 1 TO 128 (BINARY STEPS)**
- **PROGRAMMABLE DATA OUTPUT RATESUP TO 20KSPS**
- **PRECISION ON-CHIP 1.22V REFERENCE ACCURACY: 1.5%**
  **DRIFT: ±20ppm of REFOUT**
- **EXTERNAL DIFFERENTIAL REFERENCE Upto 2.5V**
- **ON-CHIP CALIBRATION**
- **SPI COMPATIBLE**
- **3.0V TO 3.6V**
- **Rad Hardened (TID) upto 300kRad**
- **SEL/SEU immune upto 50 LET MeV-cm2/mg**
- **180nm SCL CMOS standard logic process**
- **ESD Protection upto ±3KV HBM**
- **$\theta_{JC}$ =3.7°C/W**

## DESCRIPTION:

The **SC1218-0** is a precision, wide range, Sigma-Delta, Analog-to-Digital converter with 24-bit resolution operating from 3.0V to 3.6V. It has fully four differential multiplexed channels. The PGA (Programmable Gain Amplifier) provides selectable gains of 1 to 128 in binary steps with an effective resolution of 19 bits at PGA 1 and OSR of 2048. It uses a second order Sigma Delta Modulator that converts the analog input signal in to a digital pulse train whose average duty cycle represents the digitized signal information. The pulse train is then processed by a digital sinc3 filter to produce a digital output.

The decimation ratio of the digital filter can be programmed by user either to achieve higher accuracy or higher throughput. SC1218-0 has digitally on-chip offset and gain calibration. The serial interface is SPI Compatible. It can be configured to scan all the signal input sequentially with minimum communication overhead.



Notes: (1) Tested and verified upto 14 Bits.
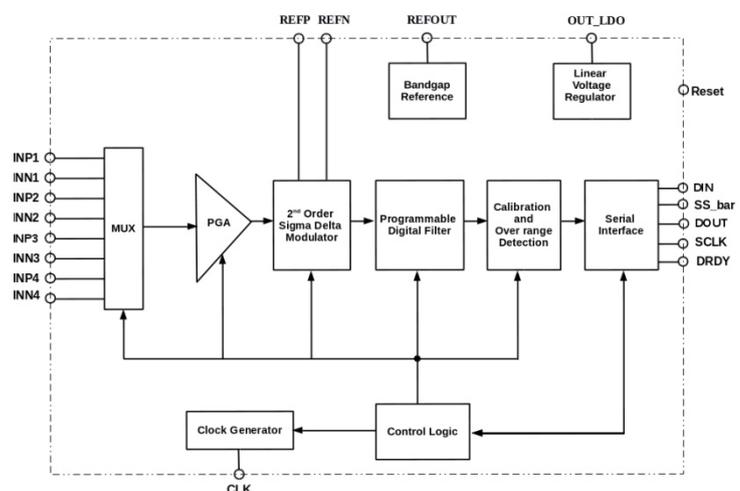
## PIN CONFIGURATION:
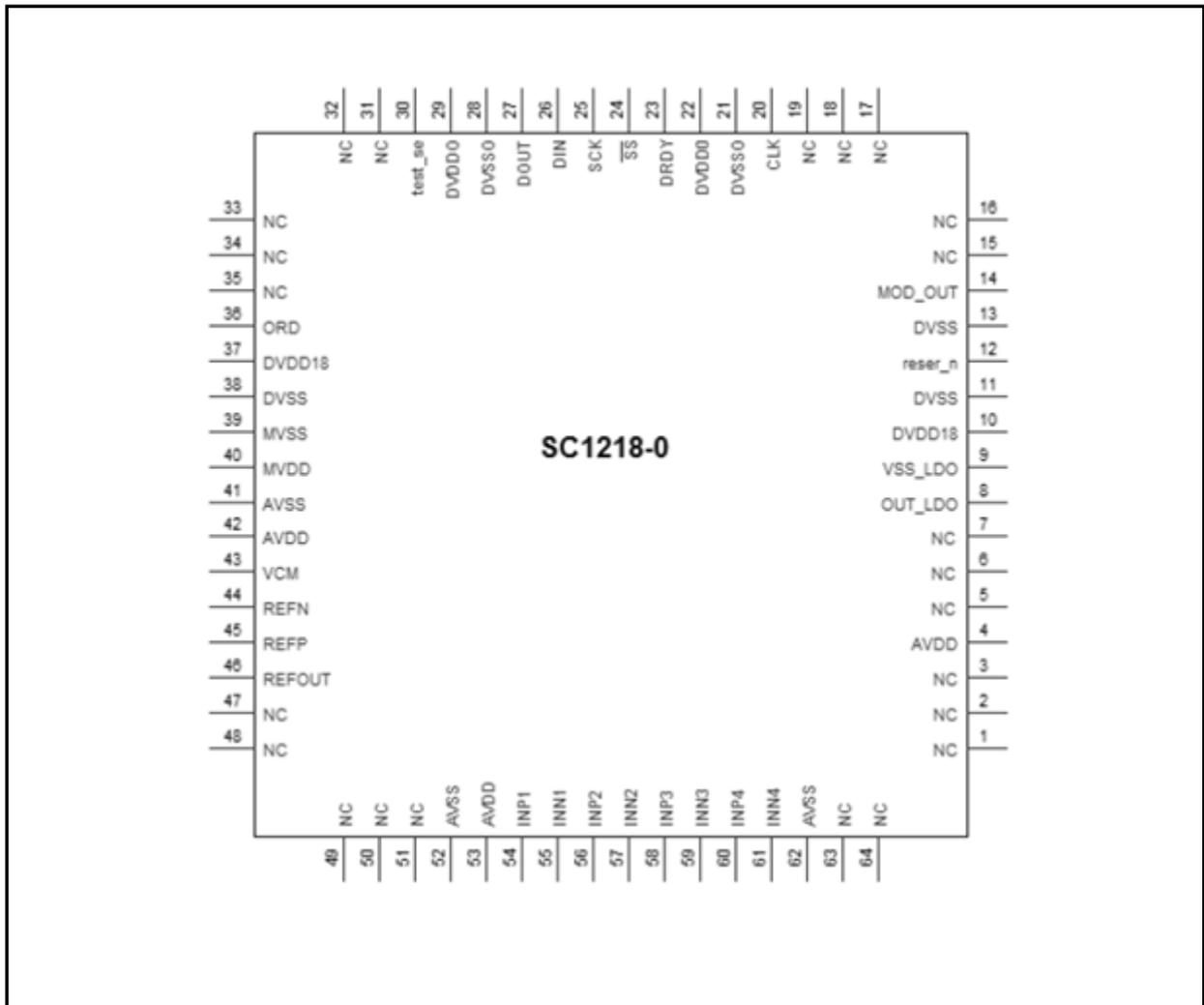


## PIN DESCRIPTIONS:

| PINNO. | NAME | DESCRIPTION |
|---|---|---|
| 1 | N.C. | Not Connected |
| 2 | N.C. | Not Connected. |
| 3 | N.C. | Not Connected |
| 4 | AVDD | Analog Core Power Supply(3.3V) |
| 5 | N.C. | Not Connected |
| 6 | N.C. | Not Connected. |
| 7 | N.C. | Not Connected |
| 8 | OUT_LDO | LDO Output (1.8V) |
| 9 | VSS_LDO | LDO Ground |
| 10 | DVDD18 | Digital Core Power Supply(1.8V) |
| 11 | DVSS | Digital Core Ground |
| 12 | reset_n | Reset ,Active Low |
| 13 | DVSS | Digital Core Ground |
| 14 | MOD_OUT | Modulator Output (Test Pin). To be kept floating |
| 15 | N.C. | Not Connected |
| 16 | N.C. | Not Connected. |
| 17 | N.C. | Not Connected |

| 18 | N.C. | Not Connected. |
|----|------|----------------|
| 19 | N.C. | Not Connected |
| 20 | CLK | Clock Input |
| 21 | DVSSO | Digital I/O ground |
| 22 | DVDDO | Digital I/O Power Supply(3.3V) |
| 23 | DRDY | Data Ready, Active Low |
| 24 | SS | Serial Interface Enable, Active Low |
| 25 | SCLK | Serial Clock |
| 26 | DIN | Serial Data Input |
| 27 | DOUT | Serial Data Output |
| 28 | DVSSO | Digital I/O ground |
| 29 | DVDDO | Digital I/O Power Supply(3.3V) |
| 30 | test_se | Scan Enable |
| 31 | N.C. | Not Connected. |
| 32 | N.C. | Not Connected |
| 33 | N.C. | Not Connected |
| 34 | N.C. | Not Connected. |
| 35 | N.C. | Not Connected |
| 36 | ORD | Over Range Detection |
| 37 | DVDD18 | Digital Core Power Supply(1.8V) |
| 38 | DVSS | Digital Core Ground |
| 39 | MVSS | Mixed Signal Ground |
| 40 | MVDD | Mixed Signal Power Supply(3.3V) |
| 41 | AVSS | Analog Core Ground |
| 42 | AVDD | Analog Core Power Supply(3.3V) |
| 43 | VCM | Common mode Voltage (1.65V) output Pin. |
| 44 | REFN | Negative Differential Reference Input |
| 45 | REFP | Positive Differential Reference Input |
| 46 | REF_OUT | Output of Band Gap Reference |
| 47 | N.C. | Not Connected. |
| 48 | N.C. | Not Connected |
| 49 | N.C. | Not Connected |
| 50 | N.C. | Not Connected. |
| 51 | N.C. | Not Connected |
| 52 | AVSS | Analog Core Ground |
| 53 | AVDD | Analog Core Power Supply(3.3V) |
| 54 | INP1 | Multiplexer Positive Input of channel1. |
| 55 | INN1 | Multiplexer Negative Input of channel1. |
| 56 | INP2 | Multiplexer Positive Input of channel2. |
| 57 | INN2 | Multiplexer Negative Input of channel2. |
| 58 | INP3 | Multiplexer Positive Input of channel3. |
| 59 | INN3 | Multiplexer Negative Input of channel3. |
| 60 | INP4 | Multiplexer Positive Input of channel4. |
| 61 | INN4 | Multiplexer Negative Input of channel4. |
| 62 | AVSS | Analog Core Ground |
| 63 | N.C. | Not Connected. |
| 64 | N.C. | Not Connected |

## TIMING SPECIFICATIONS:
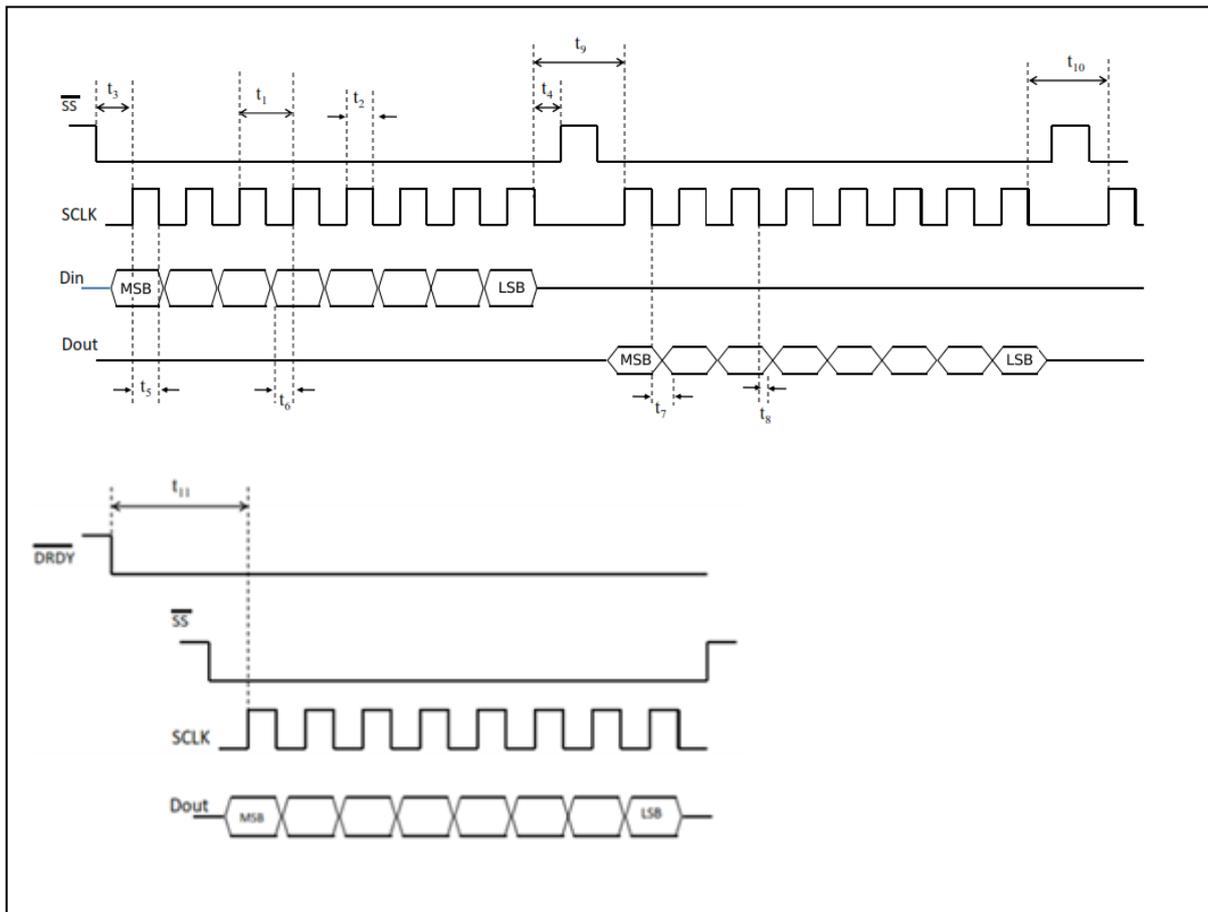


## TIMING SPECIFICATION TABLES:

| SPEC | DESCRIPTION | MIN | MAX | UNIT |
|------|-------------|-----|-----|------|
| $t_1$ | SCLK period | 4 cycle | | $t_{CLK}$ Period |
| $t_2$ | SCLK pulse width (High and Low) | 2 cycle | | $t_{CLK}$ Period |
| $t_3$ | SS low to first SCLK edge | 100 | | ns |
| $t_4$ | Last SCLK falling edge to SS HIGH | 100 | | ns |
| $t_5$ | SCK rising edge to DIN valid (Hold time) | 50 | | ns |
| $t_6$ | DIN valid to SCLK rising edge (Setup time) | 50 | | ns |
| $t_7$ | SCLK falling Edge to valid new Dout | | 50 | ns |
| $t_8$ | SCLK falling Edge to DOUT, Hold Time | 0 | | ns[2] |
| $t_9$ | Delay between last SCLK edge of 1st byte transfer and first SCLK edge for subsequent 2nd byte transfer : RDATA, RDATAC, RREG, WREG Command | 50 | | $t_{CLK}$ Period |
| $t_{10}$ | Final SCLK edge of one command until first edge SCLK of next command | 4 | | $t_{CLK}$ Period |
| $t_{11}$ | DRDY LOW to first SCLK edge of first byte transfer for RDATAC command | 15 | | $t_{CLK}$ Period |
| $t_{11}$ | DRDY LOW to first SCLK edge of first byte transfer for RDATA command | 0 | | $t_{CLK}$ Period |

Notes: (1) DOUT goes immediately into tri-state whenever SS is high (2) DOUT should be sampled externally on rising edge of SCLK. DOUT will remain valid till next falling edge.

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# ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDDO= +3.3V, DVDD18 = +1.8V, Temp. = 25ºC, OSR=2048, $f_{MOD}$ = 78.125 KHz, $f_{CLK}$ =2.5MHz, PGA=1, $f_{Data}$ = 38.147Hz, REF IN+ =2.65V, REF IN- =0.65V, unless otherwise specified.
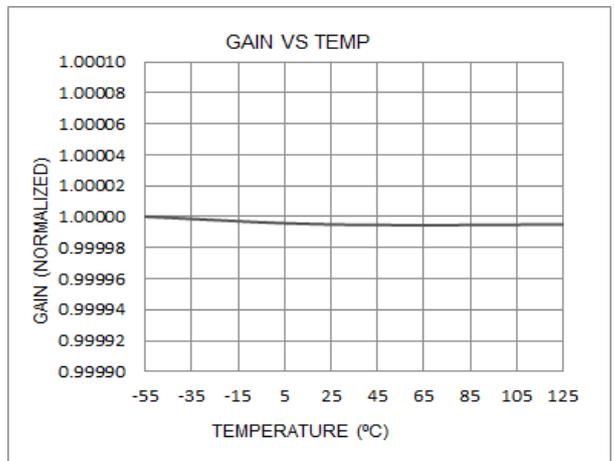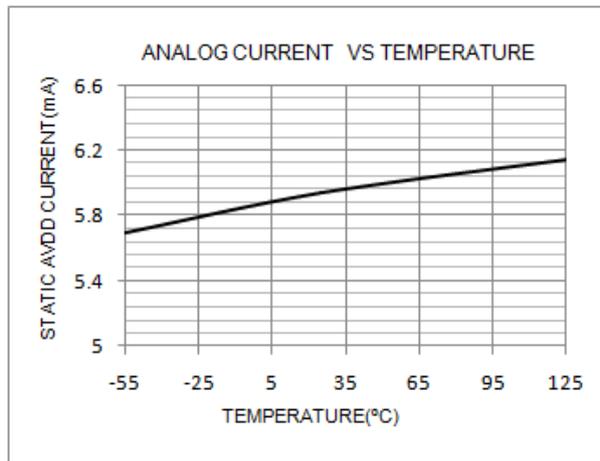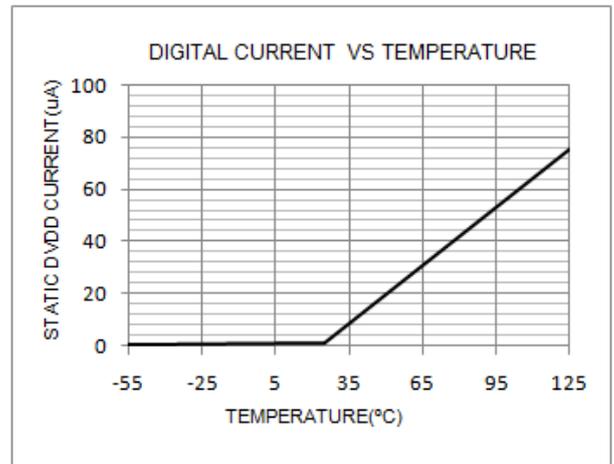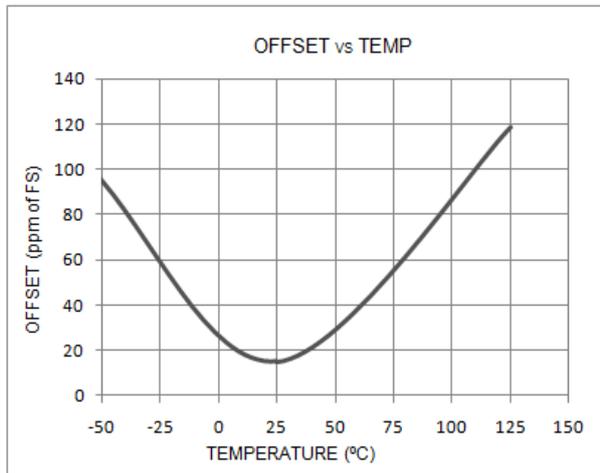
| PARAMETER | TESTS CONDITIONS | SC1218-0 | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| **ANALOG** | | | | | |
| Analog Input Range | | 0 | | AVDD | V |
| Full Scale Input Range | $V_{INP}$-$V_{INN}$ | -$V_{REF}$/PGA | | +$V_{REF}$/PGA | V |
| Programmable Gain Amplifier | User Selectable | 1 | | 128 | |
| Static Input Current | | | | 1.0 | µA |
| Input Capacitance | | | 2 | | pF |
| Bandwidth | | | | | |
| Sinc³Filter*** | -3dB | | 0.262*$f_{Data}$ | | Hz |
| Differential Input  Impedance | Modulator Frequency=78KHz | | 100 | | KΩ |
| **DEVICE PERFORMANCE** | | | | | |
| Resolution | | 24 | | | Bits |
| No Missing Code* | OSR=512,$f_{CLK}$ =5MHz,$f_{MOD}$ = $f_{CLK}$ /32 | 14 | | | Bits |
| Integral Non-Linearity | Best Fit Method | | | ±0.003 | % of FS |
| Offset Error | After Calibration | | | 25 | ppm of FS |
| Offset Drift | -55ºC to +125ºC | | | 2.5 | ppm of FS/ºC |
| Gain Error | After Calibration | | | 0.025 | % of FS |
| Gain Drift | -40ºC to +125ºC | | | 0.03 | ppm /ºC |
| Effective Resolution | Based on 100 samples | | | 19 | Bits |
| Common-Mode Rejection | At DC | | 85 | | dB |
| | $f_{CM}$=10Hz,$f_{DATA}$=30Hz | | 89 | | dB |
| | $f_{CM}$=100Hz,$f_{DATA}$=30Hz | | 89 | | dB |
| | $f_{CM}$=1KHz,$f_{DATA}$=30Hz | | 95 | | dB |
| Power Supply Rejection | DC,dB = –20 log(ΔVOUT /ΔVDD) | | 77 | | dB |
| | $V_{ac}$=±660m$V_{P-P}$, 10Hz,$f_{DATA}$=30Hz | | 58 | | dB |
| | $V_{ac}$=±660m$V_{P-P}$, 100Hz,$f_{DATA}$=30Hz | | 59 | | dB |
| | $V_{ac}$=±660m$V_{P-P}$, 1KHz,$f_{DATA}$=30Hz | | 60 | | dB |
| **ON CHIP VOLTAGE REFERENCE** | | | | | |
| Output Voltage | No Load | 1.2 | 1.22 | 1.26 | V |
| Drift | | | | ±80 | ppm/ºC |
| Start up Time** | | | | 50 | µS |
| Load Regulation | @Full Load Current = 2.5mA | | | 1.0 | % |
| **VOLTAGE REFERENCE INPUT** | | | | | |
| VREF | (REFIN+)-(REFIN-) | | 2.0 | 2.5 | V |
| **CLOCK INPUT**  $f_{CLK}$ | | | 2.5 | 20 | MHz |
| **POWER SUPPLY REQUIREMENT** | | | | | |
| Supply Voltage | AVDD, DVDDO,MVDD | 3.0 | 3.3 | 3.6 | V |
| | DVDD18 | 1.62 | 1.8 | 1.98 | V |
| Analog Current | **I_AVDD** | | 6 | 7 | mA |
| Digital Current | **I_DVDD18** | | 1000 | 1500 | µA |
| **ON CHIP LDO** | | | | | |
| Output Voltage | OUT_LDO | 1.71 | 1.80 | 1.89 | V |
| Line Regulation | | | | 1.0 | % |
| Load Regulation | @Full Load Current = 5mA | | | 1.0 | % |
| Temp Drift | -55ºC to +125ºC | | | ±200 | ppm/ºC |
| **TEMPERATURE RANGE** | | | | | |
| Operating | | -55 | | 125 | ºC |
| **Total Ionize Dose** | Upto 300KRad | | Pass | | |
| **Single Event Effect** | | | | | |
| Single Event Latch up | Upto 50 LET (MeV-cm²/mg) | | Pass | | |
| Single Event Upset | Upto 50 LET (MeV-cm²/mg) | | Pass | | |

*Missing codes are verified and tested upto 14bits. Device may perform for better results.
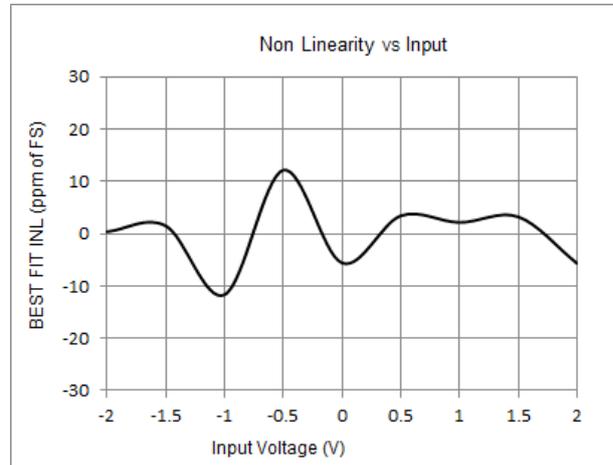**Simulated Result

# ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDDO= +3.3V, DVDD18 = +1.8V, Temp. = 25°C, OSR=2048, $f_{MOD}$ = 78.125 KHz, $f_{CLK}$ =2.5MHz, PGA=1, $f_{Data}$ = 38.147Hz, REF IN+ =2.65V, REF IN- =0.65V, unless otherwise specified.



EFFECTIVE NMBER OF BITS VS OVER SAMPLING RATIO



CMRR VS DC COMMON MODE INPUT



OFFSET vs TEMP



DIGITAL CURRENT VS TEMPERATURE
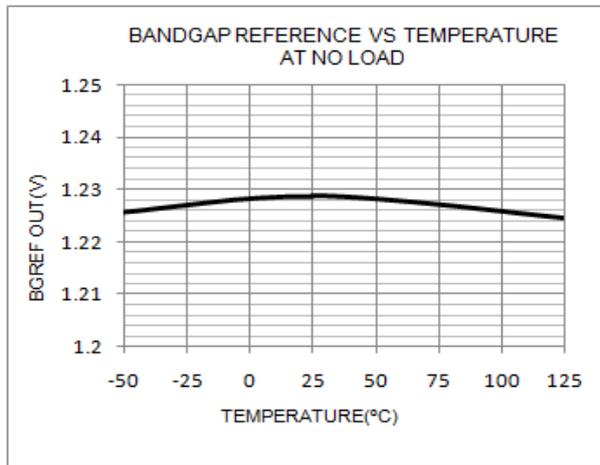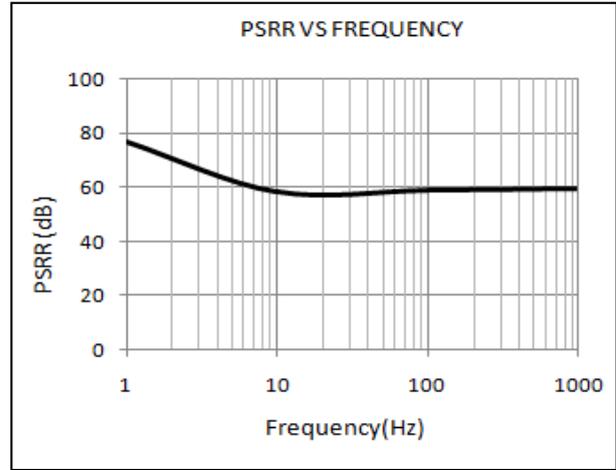


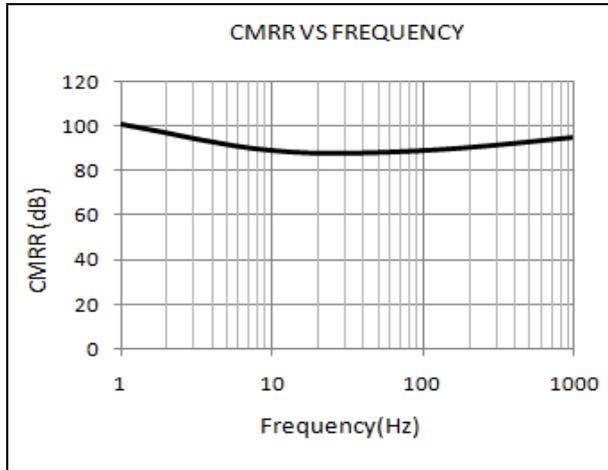ANALOG CURRENT VS TEMPERATURE



GAIN VS TEMP

# ELECTRICAL CHARACTERISTICS

All Specifications AVDD, MVDD, DVDDO= +3.3V, DVDD18 = +1.8V, Temp. = 25ºC, OSR=2048, $f_{MOD}$ = 78.125 KHz, $f_{CLK}$ =2.5MHz, PGA=1, $f_{Data}$ = 38.147Hz, REF IN+ =2.65V, REF IN- =0.65V, unless otherwise specified.

**CMRR VS FREQUENCY**

**PSRR VS FREQUENCY**

**BANDGAP REFERENCE VS TEMPERATURE AT NO LOAD**

**Non Linearity vs Input**

# DIGITAL CHARACTERISTICS

DVDDO= 3.0V to 36V

| PARAMETER | TESTS CONDITIONS | SC1218-0 | | | UNITS |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | |
| Logic Family | | | CMOS | | |
| Logic Level: $V_{IH}$ | | 2 | | DVDDO | V |
| $V_{IL}$ | | DVSS | | 0.8 | V |
| $V_{OH}$ | $I_{OH}$=8mA | 3.0 | | | V |
| $V_{OL}$ | $I_{OL}$=8mA | DVSS | | 0.4 | V |
| Input Leakage: $I_{IH}$ | $V_I$=DVDDO | | | 1 | µA |
| $I_{IL}$ | $V_I$=DVSS | -1 | | | µA |

# ABSOLUTE MAXIMUM RATING

| PARAMETER | SC1218-0 | | UNITS |
|---|---|---|---|
| | MIN | MAX | |
| AVDD to AVSS | -0.3 | 4.3 | V |
| DVDDO to DVSS | -0.3 | 4.3 | V |
| DVDD18 to DVSS | -0.3 | 2.2 | V |
| INP, INN | -0.3 | AVDD+0.3 | V |
| Digital Input Voltage to DGND | -0.3 | DVDDO+0.3 | V |

| | | | |
|---|---|---|---|
| Digital Output Voltage to DVSS | -0.3 | DVDDO+0.3 | V |
| Digital Output Current | | 8 | mA |
| Maximum Ambient Temperature | | 125 | °C |

# TEST CIRCUIT DIAGRAM



# PCB LAYOUT RECOMMENDATION

The test / application board should be four layer PCB. To achieve highest level of performance, surface-mount components to be used wherever possible. This reduces the trace length and minimizes the effects of parasitic capacitance and inductance. The board should use separate ground with all the analog signals and the digital signals. Bypass capacitors are strongly recommended at power supply and reference pins of the converter. User should also use R-C filter (49.9Ωand 47pF) on each input to have better performance.

# OVERVIEW

## INPUTMULTIPLEXER

The input analog multiplexer can select any of the four differential inputs. The output of the multiplexer is connected internally to ADC input. Analog multiplexer channel can be selected by setting MSEL1:MSEL0 bits in CR1 control register.

## PROGRAMMABLEGAINAMPLIFIER

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Adjusting the internal gain of a sigma delta modulator is a technique, which can be used to get an appropriate LSB size for the transducers application. It will improve the resolution of the ADC.  PGA gain can be selected by setting PGA2:PGA0 bits in CR1 control register.

## MODULATOR

A second order single loop sigma delta modulator is used in the Sigma Delta ADC. The sigma delta modulator converts the input signal into a digital pulse train whose average duty cycle represents the digitized signal information. The integrators used in the modulator are switched capacitor based. The first integrator of the modulator is auto-zeroed.

The modulator runs at clock frequency $f_{MOD}$ that can be adjusted by setting the appropriate value of PRE1: PRE0 of CR2 control register as shown in the following table:

| PRE1:PRE0 | $f_{MOD}$ |
|---|---|
| 00 | $f_{CLK}/16$ |
| 01 | $f_{CLK}/32$ |
| 10 | $f_{CLK}/64$ |
| 11 | $f_{CLK}/128$ |

Where $f_{CLK}$ is external clock frequency

Themodulatorisdesignedtoworkatmax imumsamplingfrequencyof*625KHz.*The output of modulator is available at MOD_OUT pin for the diagnosis purpose.

## PROGRAMMABLE DIGITAL FILTER

The on-chip digital filter processes the single bit data stream from the modulator using a sinc3 filter. The sinc filters are conceptually simple, efficient and flexible, especially where variable resolution and data rates are required. Output data rate of digital filter can be programmed by setting OSR2:OSR0 bits of CR2 control register.

| OSR2:OSR0 | Output Data Rate |
|---|---|
| 000 | $f_{MOD}/2048$ |
| 001 | $f_{MOD}/1024$ |
| 010 | $f_{MOD}/512$ |
| 011 | $f_{MOD}/256$ |
| 100 | $f_{MOD}/128$ |
| 101 | $f_{MOD}/64$ |
| 110 | $f_{MOD}/32$ |

Whenever there is step change in input or MUX selection, digital filter requires three cycles to settle.

### DRDY (DATA READY)

The DRDY pin is used as a status signal to indicate when new digital code is ready to read. DRDY goes low when new data is available. It becomes high when a read operation from the data register is executed using RDATA or RDATAC command. The DRDY pin goes high at the middle of read of

2ndMSB byte. In case, when no read operation is performed, DRDY will remain low.

## BANDGAP REFERENCE

The device has on chip 1.2V bandgap reference circuitry. To use it, the user needs to connect it externally with ADC reference pins.

## SERIAL INTERFACE

The serial interface is standard four-wire SPI compatible (DIN, DOUT, SCLK and SS).SCLK frequency can go up to $f_{CLK}$ /4. If SS pin goes HIGH the serial interface will reset and DOUT pin will become tri-state.

The SS must be LOW during the communication. DIN is the serial data input port. It is internally sampled at positive edge of SCLK by SPI. DOUT is the serial data output port and is launched at negative edge of SCLK.

SS pin can be tied low to use SPI as 3-wire interface.

## OFFSET AND GAIN CALIBRATION

Both self offset error in SC1218-0 device or complete system offset error can be reduced with offset calibration. This is handled with two offset commands SEFOCAL and SYSOCAL. There is also a gain calibration module to compensate system gain error with commands SELFGAIN and SYSGAIN. ***Please refer calibration procedure section***. Each calibration process takes five conversion cycles to complete. Calibration must be performed after system reset, a change in decimation ratio or a change of the PGA.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to apply gain correction, GCALEN bit has to be set. SELFGAIN command is only applicable at PGA1.

## OVER-LOAD DETECTION MODULE

Where digital code without calibration is such that it cannot be corrected after calibration then Over-Load detection module detects over-load and clip digital output appropriately to $7FFFFF_H$ and $800000_H$.

Status of over-load detection module is available at ORD Pin. This pin will become high in case of over-load condition.

Over-load detection can be disabled by setting OLDD flag of CR2 control register. By default it is enabled.

## OVER-RANGE DETECTION MODULE

If digital code after gain and offset calibration is out of the acceptable code range then digital over-range module detects over-range and clip digital output appropriately to $7FFFFF_H$ and $800000_H$. To ensure the proper functioning of the Over Range Detection Module, following constraint on OCR & FSR register value must be followed:

Maximum value of OCR register should not exceed $3FFFFF_H$ for negative offset correction and $C00000_H$ for positive offset correction.

FSR value must be positive.

When device is in the over-range condition, the ORD pin will become high.

Over-range detection can be disabled by setting OVDD flag of CR2 control register. By default it is enabled.

OVDD bit also affects digital output range. Setting OVDD bit will half the digital output range as shown below.

| OVDD BIT | ANALOG INPUT | DIGITAL OUTPUT CODE |
|---|---|---|
| 0 | $+V_{REF}$ | $7FFFFF_H$ |
| | 0 | $000000_H$ |
| | $-V_{REF}$ | $800000_H$ |
| 1 | $+V_{REF}$ | $3FFFFF_H$ |
| | 0 | $000000_H$ |
| | $-V_{REF}$ | $C00000_H$ |

## CALIBRATION PROCEDURE

TheSC1218-0 device has two commands namely SEFOCAL and SYSTEMOCAL to compensate offset errors. Internal calibration of device is called self calibration. By executing SELFOCAL command, the device shorts the ADC input and stores the offset value into OCR register in 2's complement form.

For system calibration, the user must apply appropriate 'zero signal' to the selected input channel and then execute SYSOCAL command. In this case ADC computes the offset value based on the available differential input signal and stores it into OCR register in 2's complement form. The System gain calibration requires appositive "full scale differential input signal. On executing system gain command, ADC computes a value to nullify gain error.

Calibration commands will only update the Offset Calibration Register (OCR) with appropriate offset value. However, to enable the offset correction, OCEN bit of CR1 control register has to be set separately. Similarly to enable gain calibration set GCALEN bit of CR1 register. Each calibration process takes five conversion cycles to complete. DRDY will be asserted to indicate completion of the calibration process.

Apart from above commands, OSR and FSR can be accessed externally through RREG (Read Register) and WREG (Write Register) commands. This will provide flexibility to manually set the OCR and FSR.

When FSR is externally loaded, follow the procedure as below.

- Perform Self/System gain calibration as sated above and read the FSR register and note down the value.
- Divide FFFFFC00000 by noted value of FSR register and take its integer portion.
- This calculated value has to be written into FSR register at next power ON in order to perform gain calibration without command.

For example:
Let noted value of FSR register is 3ee259.

The value to be written in the FSR reg. after power off and on will be:

FFFFFC00000/3ee259 = 4122B7.

# COMMAND DEFINITIONS

The commands listed below control the operation of SC1218-0 Device. Some commands are stand-alone commands (e.g. STOPC) while others require additional bytes (e.g., WREG requires command and the data bytes).

Operands:

rrrr represents the register address.

nnnnnnnn represents the data.

xxxx: these bits will be ignored while instruction decoding.

| COMMANDS | DESCRIPTION | COMMANDBYTE | 2$^{ND}$COMMANDBYTE |
|---|---|---|---|
| RDATA | Read Data | 0001 xxxx (1x$_H$) | -N.A.- |
| RDATAC | Read Data Continuously | 0010 xxxx (2x$_H$) | -N.A.- |
| STOPC | Stop Read Data Continuously | 0011 xxxx (3x$_H$) | -N.A.- |
| RREG | Read from Register rrrr | 0100rrrr(4r$_H$) | -N.A.- |
| WREG | Write to Register rrrr | 0101rrrr(5r$_H$) | nnnnnnnn |
| SELFOCAL | Self Offset  Calibration | 0110xxxx(6x$_H$) | -N.A.- |
| SYSOCAL | System Offset Calibration | 0111xxxx(7x$_H$) | -N.A.- |
| SELFGAIN | Self Gain  Calibration | 1000xxxx(8x$_H$) | -N.A.- |
| SYSGAIN | System Gain Calibration | 1001xxxx(9x$_H$) | -N.A.- |

**RREG (READREGISTER)**

RREG (Read Register) command reads content of the specified register. The address of the register to be read is specified in the LSB nibble of the instruction.
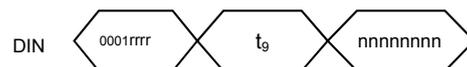
Operands: r, n
Bytes: 2
Encoding: 0100 rrrr
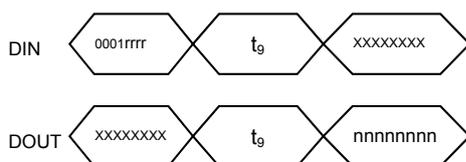


**WREG (WRITE REGISTER)**

WREG (Write Register) command writes the data to specified register. The address of the register to be written is specified in the LSB nibble of the first byte. Second byte represents the data to be written.

Operands: r, n
Bytes: 2
Encoding: 0101rrrr   nnnnnnnn



**RDATA (READDATA)**

This command reads a single 24-bitADCconversionresult.In response to RDATA command ADC transmit 24-bit digital code. Digital code is available at

DOUT pin in 8-bit format with most significant byte first. RDATA command must be followed by 3-byte read operation. On completion of read operation, DRDY goes high.
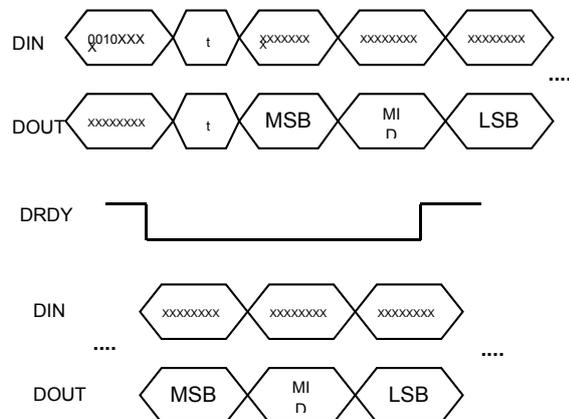
Operand: x
Bytes: 1
Encoding: 0001 xxxx
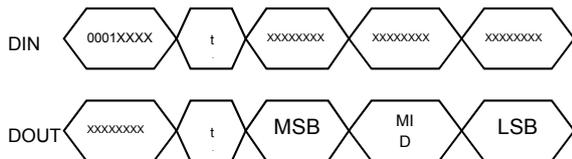


## RDATAC (READ DATA CONTINUOUS)

RDATAC command enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. In case of read data continuous command user can directly perform 3 read operation to read 24-bit digital code. DRDY will go high in response to 3-byte read operation. RDATAC command must be followed by STOPC command before issuing any other command.
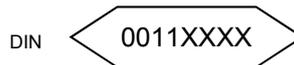
Operand: x
Bytes: 1
Encoding: 0010 xxxx



## STOPC (STOP READ DATA CONTINUOUS)

This command ends the continuous data output mode. After this command DRDY will also go high.

Operands: x
Bytes: 1
Encoding: 0011 xxxx



## SELFOCAL (SELF OFFSET CALIBRATION)

This command performs Self Offset Calibration. At the end of the calibration process, offset value will be stored in 24-bit internal Offset Calibration Register (OCR) is in 2's complement format. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 0110 xxxx
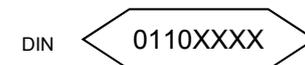


## SYSOCAL (SYSTEM OFFSET CALIBRATION)

With this command ADC computes the offset value based on the available differential input signal on selected analog channel to nullify offset in the system. The offset value will be stored in 24-bit internal Offset Calibration Register (OCR) in 2's complement format. DRDY will be asserted low to indicate completion of the command.
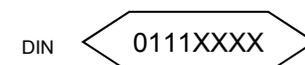
Operands: x
Bytes: 1
Encoding: 0111xxxx

## SELFGAIN (SELF GAIN CALIBRATION)

This command performs Self Gain Calibration. At the end of the calibration process, gain calibration coefficient value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.

Operands: x
Bytes: 1
Encoding: 1000 xxxx

DIN    ⟨ 1000XXXX ⟩

## SYSGAIN (SYSTEM GAIN CALIBRATION)

With this command ADC computes the gain value based on the available differential input signal on selected analog channel to nullify gain error in the system. The gain value will be stored in 24-bit internal FSR Register. DRDY will be asserted low to indicate completion of the command.
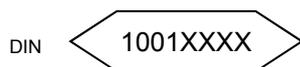
Operands: x
Bytes: 1
Encoding: 1001xxxx

DIN    ⟨ 1001XXXX ⟩

# CONTROL / STATUS REGISTERS

The operation of the device is set up through following control / status registers.

| Address | Register | BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|---|---|
| 0$_H$ | DIGITAL_CODE_B3 (R) | DC23 | DC22 | DC21 | DC20 | DC19 | DC18 | DC17 | DC16 |
| 1$_H$ | DIGITAL_CODE_B2 (R) | DC15 | DC14 | DC13 | DC12 | DC11 | DC10 | DC9 | DC8 |
| 2$_H$ | DIGITAL_CODE_B1 (R) | DC7 | DC6 | DC5 | DC4 | DC3 | DC2 | DC1 | DC0 |
| 3$_H$ | CR1 (RW) | PGA2 | PGA1 | PGA0 | OCEN | GCALEN | - | MSEL1 | MSEL0 |
| 4$_H$ | CR2(RW) | ACSEN | OLDD | OVDD | PRE1 | PRE0 | OSR2 | OSR1 | OSR0 |
| 8$_H$ | OCR1(RW) | OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |
| 9$_H$ | OCR2(RW) | OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |
| A$_H$ | OCR3(RW) | OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |
| B$_H$ | FSR1(RW) | FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |
| C$_H$ | FSR2(RW) | FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |
| D$_H$ | FSR3(RW) | FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

R: Read only registers
RW:  Read/Write registers

Note: At reset all registers are initialized to 00$_H$.

## CR1 (ADD: 03$_H$) CONTROLREGISTER-1

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|---|---|---|---|---|---|---|---|
| PGA2 | PGA1 | PGA0 | OCEN | GCALEN | - | MSEL1 | MSEL0 |

BIT 7-5:PGA2:PGA1:PGA0: Programmable
Gain Amplifier selection

| | |
|---|---|
| 000=1 | 100 = 16 |
| 001=2 | 101 = 32 |
| 010= 4 | 110 = 64 |
| 011= 8 | 111 = 128 |

Bit4: OCEN: Offset Calibration Enable bit
OCE = 1: Enable offset calibration
OCE = 0: Disable offset calibration

Bit3: GCALEN: Gain calibration Enable bit
GCALEN = 1: Enable Gain calibration
GCALEN = 0: Disable Gain calibration

Bit1-0: MSEL1: MSEL0: Analog Channel
        Selection

| | |
|---|---|
| 00 = Channel-0 | 10 = Channel-2 |
| 01 = Channel-1 | 11 = Channel-3 |

**Note:** Any update in CR1 or CR2 control register will reset modulator and digital filter. DRDY will also go high.

## CR2 (ADD: 04$_H$) CONTROL REGISTER- 2

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| - | OLDD | OVDD | PRE1 | PRE0 | OSR2 | OSR1 | OSR0 |

Bit6: OLDD: Analog over range detection
0 = Enable over-load detection.
1 = Disable over-load detection.

Bit5: OVDD: Digital over range detection
0 = Enable over-range detection.
1 = Disable over-range detection.

Bit4-2: PRE2:PRE1:PRE0: Prescaler bits

| PRE1:PRE0 | $f_{MOD}$ |
|-----------|-----------|
| 00 | $f_{CLK}$ /16 |
| 01 | $f_{CLK}$ /32 |
| 10 | $f_{CLK}$ /64 |
| 11 | $f_{CLK}$ /128 |

Bit2-0:OSR2:OSR0: OSR control bits.
    000 =   2048 OSR
    001 =   1024 OSR
    010 =   512 OSR
    011 =   256 OSR
    100 =   128 OSR
    101 =   64 OSR
    110 =   32 OSR

## OCR1 (ADD: 08$_H$) OFFSET CALIBRATION REGISTER-1
(Least Significant Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| OCR07 | OCR06 | OCR05 | OCR04 | OCR03 | OCR02 | OCR01 | OCR00 |

## OCR2 (ADD: 09$_H$) OFFSET CALIBRATION REGISTER-2
(Middle Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| OCR15 | OCR14 | OCR13 | OCR12 | OCR11 | OCR10 | OCR09 | OCR08 |

## OCR3 (ADD: 0A$_H$) OFFSET CALIBRATION REGISTER-3
(Most Significant Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| OCR23 | OCR22 | OCR21 | OCR20 | OCR19 | OCR18 | OCR17 | OCR16 |

## FSR1 (ADD: 0B$_H$) FULL SCAEE REGISTER-1
(Least Significant Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| FSR07 | FSR06 | FSR05 | FSR04 | FSR03 | FSR02 | FSR01 | FSR00 |

## FSR2 (ADD: 0C$_H$) FULL SCAEE REGISTER-2
(Middle Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| FSR15 | FSR14 | FSR13 | FSR12 | FSR11 | FSR10 | FSR09 | FSR08 |

## FSR3 (ADD: 0D$_H$) FULL SCAEE REGISTER-3
(Most Significant Byte)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| FSR23 | FSR22 | FSR21 | FSR20 | FSR19 | FSR18 | FSR17 | FSR16 |

## DIGITAL_CODE_B3 (ADD: 00$_H$) DIGITAL OUTPUT CODE
(MOST SIGNIFICANT BYTE)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| DC23 | DC22 | DC21 | DC20 | DC19 | DC18 | DC17 | DC16 |

## DIGITAL_CODE_B2 (ADD: 01$_H$) DIGITAL OUTPUT CODE
(MIDDLE BYTE)

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| DC15 | DC14 | DC13 | DC12 | DC11 | DC10 | DC09 | DC08 |

## DIGITAL_CODE_B1 (ADD: 02$_H$) DIGITAL OUTPUT CODE
(LEAST SIGNIFICANT BYTE)

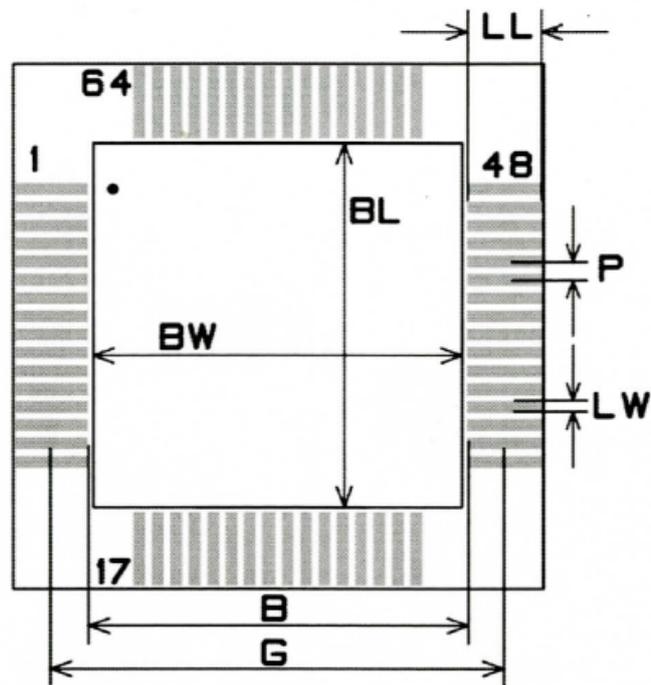| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
|------|------|------|------|------|------|------|------|
| DC07 | DC06 | DC05 | DC04 | DC03 | DC02 | DC01 | DC00 |

# PACKAGE INFORMATION

## CERAMIC QUAD FLAT PACKAGE (CQFP-64)
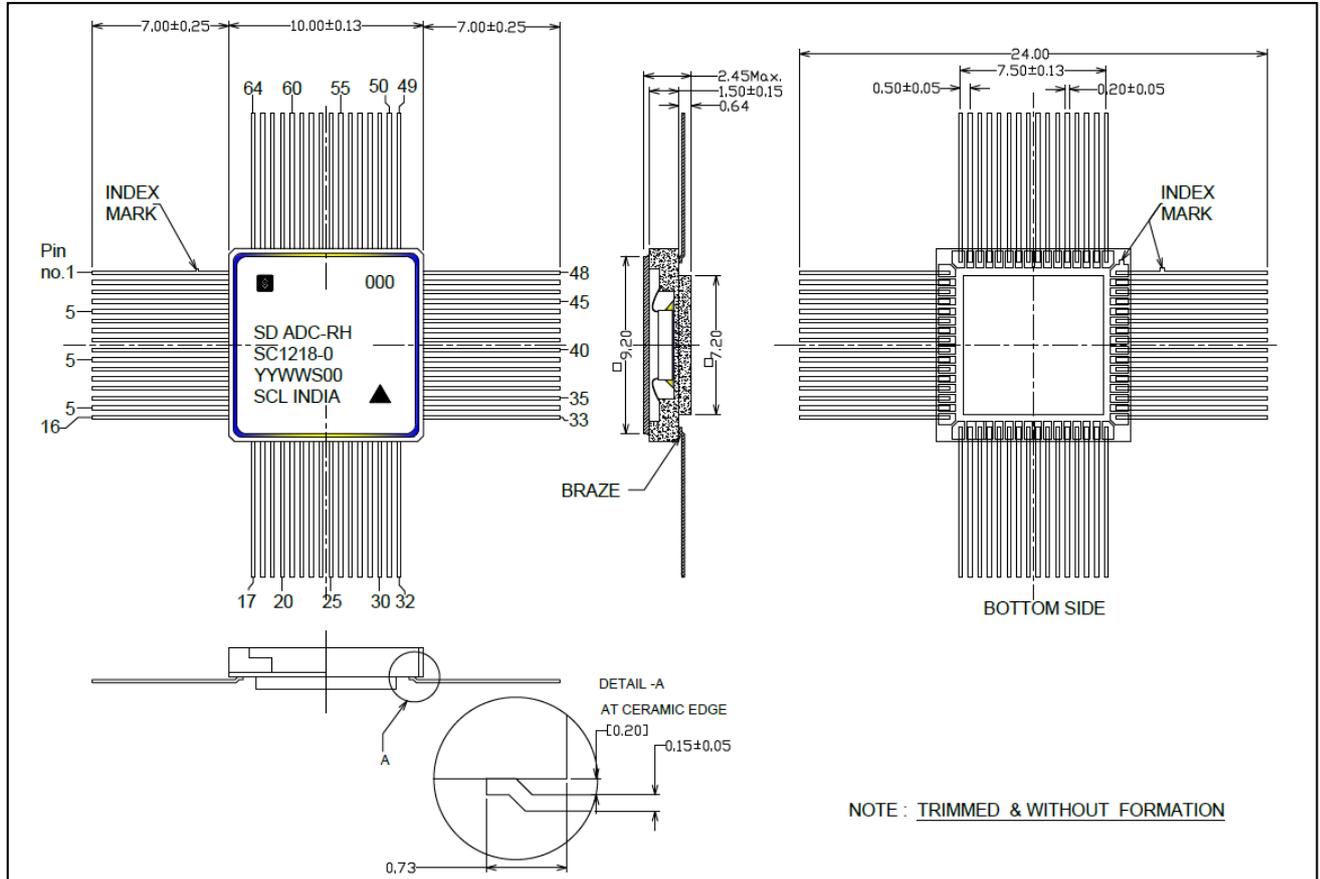


NOTE: All linear dimensions are in millimetres.

# PCB FOOTPRINT (LAND PATTERN)



| Device Drawing Title | Device Drawing Number | P | LL | LW | G | B | Part No. | Height (max.) |
|---|---|---|---|---|---|---|---|---|
| Sigma Delta ADC RH SC1218-0 (64 PIN CQFP) | A1542050170 | 0.50 | 2.60 | 0.30 | 13.4 | 10.80 | SC1218-0 | 2.45 |

Note:

1. All Dimensions are in mm
2. Device body material is ceramic
3. Device body size BL X BW is 10.13 mm x 10.13 mm (maximum)

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# TERMS AND DEFINITIONS

### Common-Mode Rejection Ratio (CMRR)

Common-mode rejection is the ability of a device to reject a signal that is common to both inputs. The Common mode signal can be an AC or DC signal, or a combination of the two. Common-mode rejection ratio (CMRR) is the ratio of the differential signal gain to the common-mode signal gain.

### Oversampling

For an ADC, sampling the analog input at a rate much higher than the Nyquist frequency is called oversampling. Oversampling improves the ADC's dynamic performance by effectively reducing its noise floor. Improved dynamic performance leads, in turn, to higher resolution. Oversampling is the basis of sigma-delta ADCs.

### Power-Supply Rejection (PSR)

Power Supply Rejection Ratio (PSRR) is the ratio of the change in DC power supply voltage to the resulting change in full-scale error, expressed in dB.

### Resolution

ADC resolution is the number of bits used to represent the analog input signal.

### Differential Nonlinearity (DNL) Error

For an ADC, the analog-input levels that trigger any two successive output codes should differ by one LSB (DNL = 0). Any deviation from one LSB is defined as DNL.

### Gain Error

The gain error of an ADC or DAC indicates how well the slope of an actual transfer function matches the slope of the ideal transfer function. Gain error is usually expressed in LSB or as a percent of full-scale range (%FSR), and it can be calibrated out with hardware or in software. Gain error is the full-scale error minus the offset error.

### Gain Error Drift

Gain-error drift is the variation in gain error due to a change in ambient temperature.

### Integral Nonlinearity (INL) Error

For data converters, INL is the deviation of an actual transfer function from a straight line. After nullifying offset and gain errors, the straight line is either a best-fit straight line or a line drawn between the endpoints of the transfer function. INL is often called 'relative accuracy.'

### No Missing Codes

An ADC has no missing codes if it produces all possible digital codes in response to a ramp signal applied to the analog input.

# TEST METHODS

**On chip reference test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Wait for 1 to 5ms. Sink zero current (or <1μA) from REFOUT pin and measure REFOUT voltage (No load Output). Fail if measured voltage is not within given limits. Similarly sink 2.5mA current from REFOUT in and measure REFOUT voltage (Full Load Output). Fail if it is not within limits. Calculate load regulation as given below

$$\text{Load Regulation} = \frac{\text{No load output} - \text{full load output}}{\text{No load Output}} * 100$$

Check the load regulation value for pass/fail limit.

**On chip LDO test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Wait for 1 to 5ms. Sink zero current (or <1μA) from OUT_LDO pin. Measure OUT_LDO voltage. Fail if measured values are not within given limits. Similarly sink 5 mA current from OUT_LDO and measure OUT_LDO voltage. Fail the measure value which is not within limits.

Load Regulation: Calculate load regulation as given below and check for pass fail/limit.

$$\text{Load Regulation} = \frac{\text{LDO output at No load} - \text{LDO output at 5mA load}}{\text{LDO output at No load}} * 100$$

Line Regulation: Apply AVDD equal to 3.0V and measure OUT_LDO voltage (VOUT1) with 5mA load current. Apply AVDD equal to 3.6V and measure OUT_LDO voltage (VOUT2) with 5mA load current.

$$\text{Line Regulation} = \frac{\text{VOUT2} - \text{VOUT1}}{(3.6 - 3.0)} * 100$$

Check line regulation value for pass/fail limit.

**Offset Error Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set OSR=2048 and $f_{MOD}$ = 78.125 KHz. Select analog channel 0 and PGA equal to 1.

Offset Error before Calibration: Apply 0V input. Read ADC data output and check for pass/fail limit.

Offset Error after self offset calibration: Perform self offset calibration. Read ADC output and checks the data for pass/fail limit.

Offset Error after system offset calibration: Perform system offset calibration. Read ADC output and check for pass/fail limit.

Repeat for all PGA setting.

**Full Scale Error Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set OSR=2048 and $f_{MOD}$ = 78.125 KHz. Enable OLDD and OVDD. Select analog channel 0 and PGA equal to 1. Perform system offset calibration.

Full Scale Error before Calibration: Apply 2V at input. Read ADC data output and check for pass/fail limit.

Full Scale Error after self gain calibration: Perform self gain calibration. Apply 2V at input and read ADC output and checks the data for pass/fail limit.

Full Scale Error after system gain calibration: Apply 2V at input. Perform system gain calibration. Read ADC output and check for pass/fail limit.

Repeat for all PGA setting.

**CMRR (Common Mode Rejection Ratio) Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set OSR=2048 and $f_{MOD}$ = 78.125 KHz. Select analog channel 0 and PGA equal to 1. Perform system offset calibration. Short channel inputs INP and INN and apply input 0V to 3.3V ($V_{CM}$) in step of 0.3V with reference to AGND. Read ADC data output for 20 samples at each step and record average value. Calculate the CMRR as given below.

$$CMRR = -20 * (Log10 ((|ADCOUT_0 - ADCOUT_{VCM}|) / V_{CM}))) + (20 * (Log10 (PGA))$$

Where $ADCOUT_0$ is average value of ADC output at 0V input and $ADCOUT_{VCM}$ is average value of ADC output at desire common mode input voltage. Check the calculated CMRR value for pass/fail limit. Repeat the procedure for all PGA setting.

**Effective Resolution Test:** Apply AVDD, DVDDO and MVDD equal to 3.3V. Apply DVDD18 equal to 1.8V. Apply reference supply 2V (REFP-REFN), clock 2.5MHz. Set $f_{MOD}$ = $f_{CLK}$ /32. Select analog channel 0 and PGA equal to 1. Perform system offset and system gain calibration. Short INP1 and INN1 and apply 1.65V w.r.t. AVSS and read ADC output for 100 samples at each PGA and OSR combinations. Calculate ENOB as given below.

$$ENOB = 24 - Log_2 (ADCOUT_{MAX} - ADCOUT_{MIN}) + 2.7$$

Where **ADCOUT_{MAX}** and **ADCOUT_{MIN}** are maximum and minimum ADC output sample value. Check the calculated ENOB for pass/fail limit.